

WHAT IS CLAIMED IS:

1. A hybrid integrated circuit (IC) package substrate, at least comprising:
 - a plurality of patterned conductive layers stacked over each other, wherein the outermost patterned conductive layer furthermore has a plurality of bonding pads
 - 5 thereon;
 - a plurality of dielectric layers respectively sandwiched between a pair of neighboring patterned conductive layers, wherein at least one of the dielectric layer is a ceramic dielectric layer and at least one of the remaining dielectric layers is an organic dielectric layer; and
- 10 a plurality of vias respectively passing through at least one of the dielectric layer for connecting at least two of the patterned conductive layers electrically.
2. The hybrid IC package substrate of claim 1, wherein one of the dielectric layers is a dielectric core layer, and the dielectric core layer is the ceramic dielectric layer.
- 15 3. The hybrid IC package substrate of claim 2, wherein the dielectric layers are symmetrically distributed on each side of the dielectric core layer.
4. The hybrid IC package substrate of claim 2, wherein the dielectric layers are non-symmetrically distributed on each side of the dielectric core layer.
5. The hybrid IC package substrate of claim 1, wherein all the remaining dielectric layers are positioned on one side of the ceramic dielectric layer.
- 20 6. A chip package structure, at least comprising:
 - a hybrid integrated circuit (IC) carrier having a first surface and a second surface, wherein the hybrid IC carrier at least having:

a plurality of patterned conductive layers stacked over each other,
wherein the patterned conductive layer closest to the first surface furthermore
has a plurality of bonding pads thereon;

5 a plurality of dielectric layers respectively sandwiched between a pair of
neighboring patterned conductive layer, wherein at least one of the dielectric
layer is a ceramic dielectric layer and at least one of the remaining dielectric
layers is an organic dielectric layer; and

10 a plurality of vias passing through at least one of the dielectric layer for
connecting at least two of the patterned conductive layers electrically; and
a chip attached to the first surface of the hybrid IC carrier and connected
electrically to the hybrid IC carrier via the bonding pads.

7. The chip package structure of claim 6, wherein one of the dielectric layers is a
dielectric core layer, and the dielectric core layer is the ceramic dielectric layer.

8. The chip package structure of claim 7, wherein the dielectric layers are
15 symmetrically distributed on each side of the dielectric core layer.

9. The chip package structure of claim 7, wherein the dielectric layers are non-
symmetrically distributed on each side of the dielectric core layer.

10. The chip package structure of claim 6, wherein all the remaining dielectric
layers are positioned on one side of the ceramic dielectric layer.

20 11. The chip package structure of claim 6, wherein the chip is electrically
connected to the hybrid IC carrier through a flip chip bonding or a wire bonding
process.

12. The chip package structure of claim 6, wherein the package furthermore
comprises a plurality of contacts attached to the second surface of the hybrid IC carrier.